AMENDMENTS TO THE CLAIMS

1. (Original) A microprocessor system comprising:

an address generator configured to simultaneously generate a first memory address and a second memory address;

a memory system having a first memory tower and a second memory tower; and

an address selector coupled to receive the first memory address and the second memory address and configured to select a first row address for the first memory tower and a second row address for the second memory tower.

2. (Original) The microprocessor system of claim 1, wherein the first row address is equal to a row portion of the first memory address, and the second row address is equal to a row portion of the second memory address.

3. (Original) The microprocessor system of claim 1, wherein the first row address is equal to a row portion of the second memory address, and the second row address is equal to a row portion of the first memory address.

4. (Original) The microprocessor system of claim 1, wherein the address generator further comprises: a first adder for generating the first memory address; and a second adder for generating the second memory address.

5. (Original) The microprocessor system of claim 4, wherein the first adder adds a first address operand and a second address operand.

6. (Original) The microprocessor system of claim 5, wherein the second adder adds the first address operand, the second address operand, and a carry bit.

7. (Original) The microprocessor of claim 5, wherein the second adder adds a portion of the first address operand, a portion of the second address operand, and a carry bit.

8. (Original) The microprocessor system of claim 1, wherein the second memory address is one memory row greater than the first memory address.

9. (Original) The microprocessor system of claim 1, wherein the second memory address has a row portion that is one greater than a row portion of the first memory address.

10. (Original) The microprocessor system of claim 1, wherein the second memory address is equal to a row portion of the first memory address plus 1.

11. (Original) The microprocessor system of claim 1, further comprising a data aligner coupled to the memory system.

12. (Original) The microprocessor system of claim 1, wherein the memory system further comprises a third memory tower and a fourth memory tower.

13. (Original) The microprocessor system of claim 8, wherein the address selector is configured to select a third row address for the third memory tower and a fourth row address for the fourth memory tower.

14. (Original) The microprocessor system of claim 1, wherein the address selector is controlled by one or more bits of the first memory address.

15. (Original) The microprocessor system of claim 1, wherein the first row address is equal to a row portion of the first memory address.

16. (Original) The microprocessor system of claim 11, wherein the second row address is equal to a row portion of the second memory address.

17. (Original) A method of accessing a memory system having a plurality of memory towers, the method comprising:

simultaneously generating a first memory address and a second memory address;

selecting a row portion of the first memory address as a first row address for a first memory tower; and

selecting a row portion of the second memory address as a second row address for a second memory tower.

18. (Original) The method of claim 17, further comprising: performing a memory access using both the first row address and the second row address.

19. (Currently Amended) The method of claim 17, wherein the simultaneously generating a first memory address and a second memory address further comprises:

adding a first memory operand and a second memory operand to generate the first memory address; and

adding the first memory operand, the second memory operand, and a carry bit to generate the second memory address.

20. (Original) The method of claim 19, wherein the carry bit is at a bit position equivalent to a row width.

21. (Currently Amended) The method of claim 17, wherein the simultaneously generating a first memory address and a second memory address further comprises:

adding a first memory operand and a second memory operand to generate the first memory address; and

adding a row portion of the first memory operand, a row portion of the second memory operand, and a carry bit to generate the second memory address.

22. (Original) The method of claim 17, wherein the row portion of the second memory address is the same as the second memory address.